

HYBRID BULK/SILICON-ON-INSULATOR MULTIPROCESSORS

ABSTRACT OF THE DISCLOSURE

A multiprocessor integrated circuit is disclosed. A preferred embodiment of a multiprocessor chip has microprocessors formed on silicon-on-insulator regions and dynamic random access memory level-2 cache memories or level-3 cache memories formed on bulk regions of the chip. A preferred embodiment includes a redundant architecture having a signal bus for coupling the microprocessors to the level-2 or level-3 cache memories in which the signal bus includes a programmable selector circuit for bypassing defective microprocessors or defective level-2 or level-3 cache memories.